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OVER-CURRENT PROTECTION CIRCUIT

Field of the Invention

The present invention relates to voltage regulators such as low drop out (LDO) voltage regulators. More particularly, the present invention relates to a method and apparatus for providing over-current protection in a voltage regulator while minimizing power losses, while also minimizing possible device failure.

Background of the Invention

Many modern analog circuits include power management systems that are arranged to provide protection and performance functions. One protection function is referred to as over-current protection. Over-current protection is typically required when a short-circuit condition occurs in the output of a circuit such as a voltage regulator. The over-current protection function can be accomplished by monitoring the current delivered to a load, and clamping the current when the system detects that it has exceeded some maximum level.

An example voltage regulator with over-current protection circuit (100) is illustrated in FIGURE 1. Circuit system 100 includes seven p-type field effect transistors (FETs P0 – P6), two n-type field effect transistors (FETs N1 – N2), an error amplifier, seven resistors (R1 – R7), a capacitor (Co), and two switches (SW1, SW2).

During operation, circuit 100 is operated from a VCC power supply. Reference currents (IREF1, IREF2) are applied to diode connected transistors P3 and P6 respectively. A reference voltage (VREF) is applied to the inverting input of the error amplifier. Resistors R3 and R4 are connected to the output load (R5, Co) to provide a feedback voltage to the non-inverting input of the error amplifier. Transistor P0 delivers an output current (IOUT) to the load (R5, Co), which is replicated by transistor P1. Transistor P3 senses the output voltage to bias transistor P4. Transistors P5 and P6 are arranged to provide a short circuit threshold voltage (VSC) to the gate of transistor P2 and the control terminal of switch SW1. During normal operation, the feedback voltage from resistors R3 and R4 is used to regulate the output voltage

(VOUT) across the load (R5, Co) by limiting the output current level (IOUT) via control of the gate voltage of transistor P0.

A short-circuit condition is simulated by the closing of a switch (SW2), which shorts the load (R5, Co) to the circuit ground. Transistor P3 senses the collapsing output voltage from the short-circuit condition and changes the operating current of transistor P4. Transistor N1 senses the current of transistors P1 and P4 and pulls down (via transistor N2) on the short-circuit threshold voltage (VSC) such that transistor P2 is enabled. The regulator output current (IOUT) is clamped to a maximum level at 3 times of its maximum load current normally.

Brief Description of the Drawings

Non-limiting and non-exhaustive embodiments of the present invention are described with reference to the following drawings.

FIGURE 1 is an illustration of a conventional voltage regulator that includes over-current protection.

FIGURE 2 is an illustration of a voltage regulator system that is arranged in accordance with an example of the present invention.

FIGURE 3 is an illustration of example signal waveforms for the circuit illustrated in FIGURE 2.

Detailed Description of the Preferred Embodiment

Various embodiments of the present invention will be described in detail with reference to the drawings, where like reference numerals represent like parts and assemblies throughout the several views. Reference to various embodiments does not limit the scope of the invention, which is limited only by the scope of the claims attached hereto. Additionally, any examples set forth in this specification are not intended to be limiting and merely set forth some of the many possible embodiments for the claimed invention.

Throughout the specification and claims, the following terms take at least the meanings explicitly associated herein, unless the context clearly dictates otherwise. The meanings identified below are not intended to limit the terms, but

merely provide illustrative examples for the terms. The meaning of "a," "an," and "the" includes plural reference, the meaning of "in" includes "in" and "on." The term "connected" means a direct electrical connection between the items connected, without any intermediate devices. The term "coupled" means either a direct electrical connection between the items connected or an indirect connection through one or more passive or active intermediary devices. The term "circuit" means either a single component or a multiplicity of components, either active and/or passive, that are coupled together to provide a desired function. The term "signal" means at least one current, voltage, charge, temperature, data, or other signal.

Briefly stated, the invention is related to an apparatus and method for providing over-current protection in a regulator system. The regulator system includes a power device and a sense device. During a normal operating mode, a power device is arranged to deliver current to a load, while the sense device is arranged to monitor the load current. An over-current mode is activated when the sensed load current exceeds a short-circuit current-limit. During the over-current mode, the power device is switched off such that the energy loss is minimized. Once the short-circuit condition is removed, the regulator system returns to the normal operating mode. The sense device is coupled to the load in such a way that the quiescent current of the regulator system does not rise with increasing load current. The regulator system is further arranged such that the short-circuit current-limit decreases automatically with increased operating temperature. The described regulator system has significantly reduced energy losses while also minimizing risks of thermal induced device failures during the short-circuit condition.

FIGURE 2 is an illustration of a voltage regulator system (200) that is arranged in accordance with an example of the present invention. Regulator system 200 comprises: an error amplifier circuit (EA), a power device (P0), a feedback circuit (R2, R3), a switch circuit (SW1), and an over-current protection circuit. The over-current protection circuit comprises: a comparator circuit (CMP), nine transistors (P1 - P5, and N0 - N3), and two resistors (R1, R4). The load circuit is represented as a resistor (RL) that is coupled in parallel with a capacitor (CL).

Circuit 200 is operated from a VCC power supply and a circuit ground (GND). Reference currents (IREF1, IREF2) are applied to diode connected transistors N1 and P5 respectively. A reference voltage (VREF) is applied to the inverting input of the error amplifier circuit (EA). Resistors R2 and R3 are connected to the output load (RL, CL) to provide a feedback voltage (e.g., VFB) to the non-inverting input of the error amplifier. Transistor P0 delivers an output current (IOUT) to the load (RL, CL), which is replicated by transistor P1. Switch circuit SW1 is operated in a closed position when the VSC signal is de-asserted and an open position when the VSC signal is asserted. However, switch circuit SW1 may not be necessary when error amplifier circuit EA is designed to include an output stage with a passive type of pull-down circuit.

Power device P0 is the main power device that is principally responsible for delivering current to the load during a normal operation mode of regulator system 200. Transistor P1 and resistor R1 are arranged to operate as a current sense circuit that senses the output current that is delivered to the load, where a first sense voltage (VSNS1) is developed across resistor R1. Transistor N0 is arranged to operate as a level shifter that translates the first sense voltage (VSNS1) to a second sense voltage (VSNS2) that is coupled to an input of comparator circuit CMP (e.g., V-). Another input of comparator circuit CMP (e.g., V+) is coupled to the output (VOUT). Comparator circuit CMP is arranged to provide a short-circuit detection signal (VSC) when the short circuit condition is detected.

Transistor P2 is arranged to deactivate power device P0 and sense transistor P1 when the short-circuit condition is detected by the current sense circuit (transistor P1 and resistor R1). Transistors P4 and P5 are arranged in a current-mirror configuration to operate as a current source that provide a current to charge the output capacitor (CL) and load after the short-circuit condition is removed. Transistor P3 is arranged to enable the current source from transistors P4 and P5 when comparator circuit CMP asserts the VSC signal. One or more inverting circuits can be placed between the output of the comparator circuit (CMP) and the VSC signal to provide increased gain and/or changing the polarity of the control signal as may be required in

other implementations. The current from transistor P4 is delivered to the load circuit (RL, CL) such that the output voltage (VOUT) increases after the short-circuit condition is removed. The level associated with the current from transistor P4 is related to the relative sizes of transistors P4 and P5, and to reference current level IREF2.

Transistors N1 and N2 are arranged in a current-mirror configuration to operate as a current source for transistor N0. Transistor N0 has a drain that is coupled to the output of the comparator (signal VSC), a gate that is coupled to the drain of transistor P1, and a source that is coupled to the drain of transistor N2. Transistor N3 is configured to maintain the inverting input (V-) of comparator circuit CMP at a level that is higher than the non-inverting input (V+) of the comparator during the short-circuit condition. The relative sizes (e.g., W/L ratio for a FET) of transistors N3 can be selected as smaller than that of transistors N1 and N2 to ensure proper operation. The short circuit current limit can be adjusted by selection of transistor sizes for transistors P1, N0 and N2, and the value associated with resistor R1. The sense current from transistor P1 flows to the output rather than the circuit ground, which provides for a reduction in power loss from wasted current.

For the example circuit illustrated in FIGURE 2, transistor P3 is illustrated as a p-type field effect transistor (PFET) such that the VSC signal is asserted as an active low signal. However, other transistor configurations may be used such that the VSC signal is asserted as an active high signal.

An example comparator circuit (CMP) is illustrated as seven transistors (P6 - P9, and N4 - N6), configured as a two-stage comparator. Transistors P6 and P9 are biased to operate as current sources. In one example, transistors P6 and P9 are biased with a common biasing signal (e.g., BIAS). In another example, transistors P6 and P9 are biased with different biasing signals (e.g., BIAS1 and BIAS2). Transistors P7 and P8 are arranged to cooperate with transistor P6 to operate as a differential pair circuit with p-type transistors in the first stage. The positive input (V+) of the comparator circuit (CMP) is coupled to regulator output (OUT) such that V+ = VOUT. The negative input of the comparator (V-) is coupled to the source of transistor N0, which is the level shifter transistor.

The mathematical relationship between various signals is described as follows:

$$V- = Vout + Is*R1 - Vgs(N0) \quad \text{(Eq. 1)}$$

$$Vgs(N0) = VTN + [(2L/W)_{N0}*Iref1/(\mu nCox)]^{1/2} \quad \text{(Eq. 2)}$$

, where Is corresponds to the sense current that flows through transistor P1 and resistor R1, VTN corresponds to a threshold voltage, $(L/W)_{N0}$ corresponds to an inverse of the size of transistor N0, μn corresponds to a mobility factor of electron, Cox corresponds to the oxide capacitance, and Vgs(N0) corresponds to the gate-source voltage of transistor N0.

In one example implementation, the sizes of transistor P0 and P1 are related to one another by a scaling factor (m) such that $(W/L)_{P0} = m*(W/L)_{P1}$. For this example, the short circuit current limit at which the comparator changes states corresponds to:

$$Isc = m*Is = m*Vgs(N0)/R1 \quad \text{(Eq. 3)}$$

During the normal operating mode of regulator system 200, VSC equals Vcc (e.g., active high) and transistor N2 is arranged to operate in its active region such that transistor N3 is deactivated (off state). In general, Vgd(N0) = Vout + Is*R1 – Vcc. Transistor N0 is operated in its active region when Vgd(N0) < VTN. The current flowing through transistors N0 and N2 is constant (Iref1) such that Vgs(N0) is also a constant. The output voltage in normal operation is regulated such that it is also a constant (as an example of approximately 1V). As the sense current (Is) increases, the inverting input voltage (V-) will also increase. The output signal (Vsc) from the comparator circuit (CMP) will remain high until the first sense voltage (VSNS1) from current (Is) reaches a level given by Is*R1 ≈Vgs(N0). Once the first sense voltage exceeds the gate-source threshold requirements of transistor N0 (Is*R1 > Vgs(N0)) the short-circuit detection signal is asserted (e.g., active low) by the comparator circuit (CMP) and transistors P0 and P1 are deactivated (completely switched off). Once transistors P0 and P1 are deactivated, the output voltage (Vout or V+) will begin to immediately decrease such that transistor N0 is deactivated (turned-off) and both V+

and V- drop "low" (e.g., to nearly the circuit ground potential). Transistors P3 and N3 will become active at the same time when the short-circuit detection signal is asserted such that transistor P4 will provide a constant current to the output. The output current from transistor P4 is relatively small and cannot cause a substantial increase in the output voltage (VOUT) while the short-circuit condition persists. Transistor N3 is arranged to increase the voltage of the inverting input (V-) at Vmin_OD during the short circuit condition such that it is always above the ground potential (e.g., a few milli volts, for example 2 mV above ground). Since the output voltage is below the inverting input voltage (V- is still higher than V+) the short-circuit detection signal (VSC) remains asserted (e.g., active low) while the short circuit condition exists. Thus, during the short-circuit condition, transistors N1 and N3 are operated in their active states, while transistor N2 operates in its linear region.

The size (W/L) of transistor N3 can be adjusted to change the amount of signal difference between the inverting input (V-) of the comparator circuit (CMP) and the ground potential. An example transistor size for a 2mV difference is described roughly based on the following relationships during a short circuit condition:

$$\begin{aligned}
&Ids(N3) = Ids(N2)\\
&Ids(N1) + Ids(N3) = Iref1\\
&Vds(N2) = 2\ mV\\
&Vgs(N3) = Vgs(N2) - 2\ mV\\
&2mV = Vgs(N2) - Vgs(N3) \qquad \text{(Eq. 4)}
\end{aligned}$$

In one example process, the relative size (W/L) of transistors N2 and N3 is determined such that transistor N3 has a relative size that is estimated to be 1/20th of that for transistors N1 and N2. However, other size ratios between transistors N2 and N3 are also contemplated such as 5:1, 10:1, 15:1, as may be required by other operating parameters that are specific to a particular semiconductor process.

Once the short-circuit condition is removed, the current flowing from transistor P4 begins to charge capacitor CL and load resistor RL. The time required for V+ to be charged to over Vmin_OD (an example of 2 mV) is approximately given by:

$$t = CL*Vmin\_OD/(I_{DP4} - Vmin\_OD/RL) \quad \text{(Eq. 5)}$$

, where RL = Vout/Imax, and Imax is the maximum output (load) current for the regulator system. It is observed from Eq. 5 that $I_{DP4} > 0.002*Imax/Vout = 0.2mA$ when the regulated output voltage (VOUT) is 1V, Vmin_OD is 2mV, and the maximum output current (Imax) is 100mA. Based on these conditions, the relative sizes of transistors P4 and P5 can be determined. The size of P3 may be set as greater than or equal to that of transistor P4. After time period t, the output voltage (V+, VOUT) is higher than inverting input (V-) and the short-circuit detection signal (Vsc) is de-asserted (e.g., returns to a high signal).

The above-described circuit arrangement returns the regulator system to a normal operating mode automatically once the short-circuit condition terminates. The turn-off for power device under short-circuit condition is useful in reducing thermal related damage to the system. For example, transistor P0 may become damaged because of thermally induced metal fatigue, etc. The total quiescent current required for supplying the above described over-current protection circuit can be minimized with careful design considerations. In one example, the total quiescent current is about 0.8μA during normal operation.

FIGURE 3 is an illustration of example signal waveforms (300) for circuit 200 illustrated in FIGURE 2. Various time periods (T1 – T5) are labeled on FIGURE 3 to illustrate the various operating modes that are contemplated in circuit 200.

During time-period T1 (disable), the regulator is inactive (disabled) such as during a power-on reset condition. The short circuit detection signal (VSC) increases to the nominal operating level (Vcc, active high) during this time-period, while the output current (IOUT) is approximately zero since transistor P0 is disabled, resulting in an output voltage (VOUT) that is collapsed to the circuit ground potential.

During time period T2 (normal operation), the regulator is active in a normal operating mode where no short-circuit condition is present in the system.

Output current (IOUT) is delivered to the load circuit (RL, CL) developing an output voltage (VOUT) as shown in the FIGURE.

During time period T3 (short circuit), a short circuit condition is applied across the load circuit (RL, CL). In the present invention as illustrated in FIGURE 2, the output current (IOUT) drops to approximately zero (neglecting the current from transistor P4 since it is very small by design), while the output current in the prior art implementation (See FIGURE 1) increases to a clamped level as illustrated by OLD IOUT. Similarly, the output voltage in the present invention decreases to approximately the circuit ground potential while the prior art circuit may have a non-zero voltage as illustrated by OLD_VOUT. The short-circuit detection signal in the present invention is coupled to a potential of approximately ground, while the prior art implementation from FIGURE 1 results in a potential that is a non-ground potential.

Time period T4 (normal operation) illustrates that circuit 200 returns to a normal operating mode after the short circuit condition is removed. As described previously, transistor P4 provides a current to the output when the short-circuit condition is removed such that the output voltage (VOUT) increases sufficient to re-enable power device P0 via the operation of comparator circuit CMP and transistor P2.

Time period T5 (disable) illustrates that circuit 200 may be disabled at a later time where regulation is no longer desired (e.g., a sleep mode or power conservation mode).

In one example implementation, VOUT decreases to potential of 0V during the short-circuit condition and IOUT decreases down to a current of approximately 200uA. In contrast, a prior art implementation such as that illustrated in FIGURE 1 has a clamped output current on the order of 330mA.

As observed by the above described differences in short-circuit operation, the thermal generation is high in the conventional circuit while very low in the present invention. By switching off the power device during the short-circuit mode, energy loss during short-circuit operation is greatly reduced. Once the short-circuit condition is removed, the protection circuit of the present invention allows the regulator to automatically return to normal operation. The currents from the sense circuit are

provided directly to the output rather than the circuit ground so that the quiescent current of the regulator does not rise with increased load current. The circuit arrangement of the present invention provides for a decreased short circuit current limit as temperature increases, providing yet further protection to the various circuits. The novel protection circuit of the present invention results in significant reductions in energy loss and reduces risks of any thermal induced device failure during short circuit operation.

The above specification, examples and data provide a complete description of the manufacture and use of the composition of the invention. Since many embodiments of the invention can be made without departing from the spirit and scope of the invention, the invention resides in the claims hereinafter appended.